CHEN, et al. 1/29 POU920000124US1

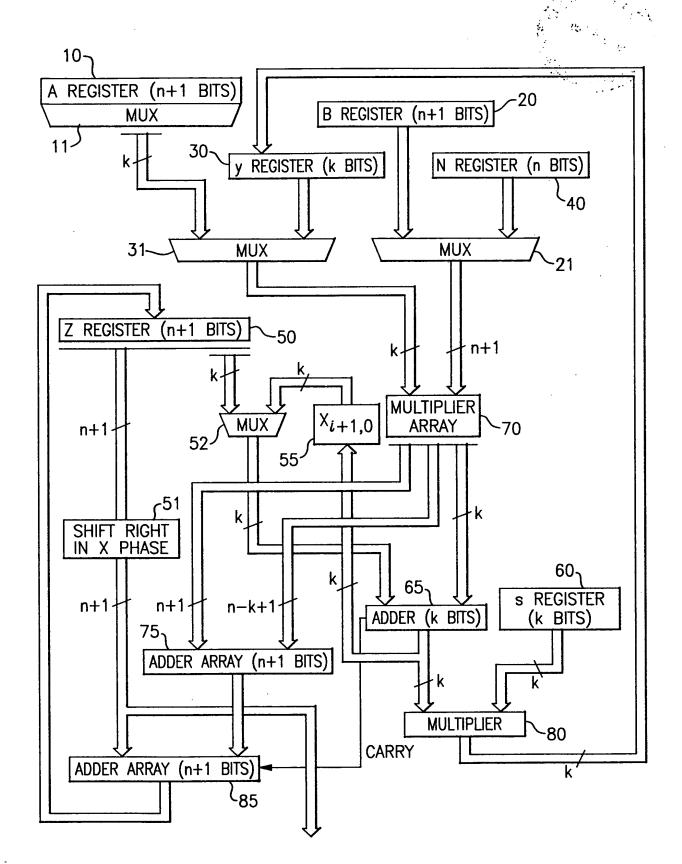


FIG.1

10-

11

n+1

n+1

 $X_i = Z_i + A_i B$

SHIFT RIGHT IN X PHASE

ADDER ARRAY (n+1 BITS)

MUX

FIG.2

CARRY

MULTIPLIER

 $y_i = sX_{i,0} \overline{MOD} R$

ADDER ARRAY (n+1 BITS)

 $A_{\boldsymbol{i}}B$

⁽85

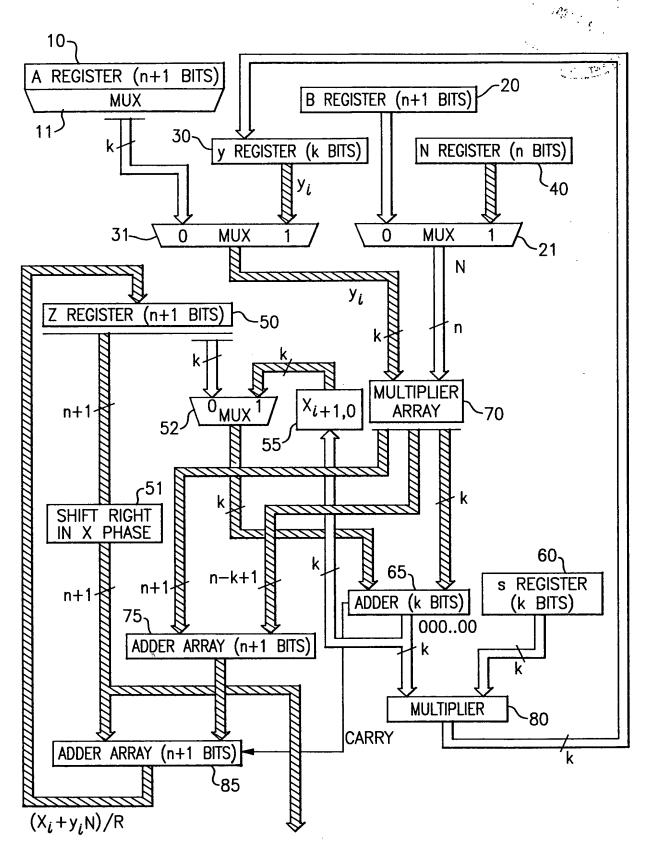


FIG.3

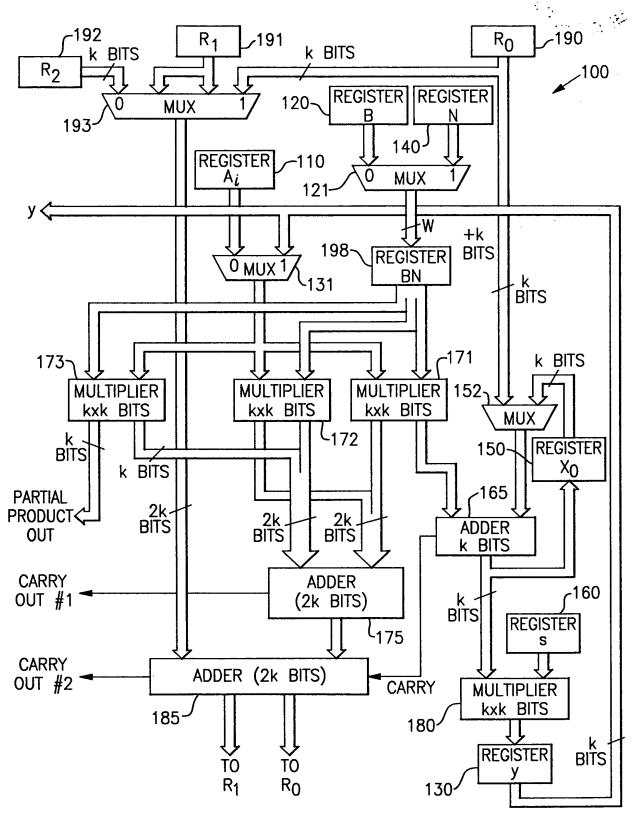
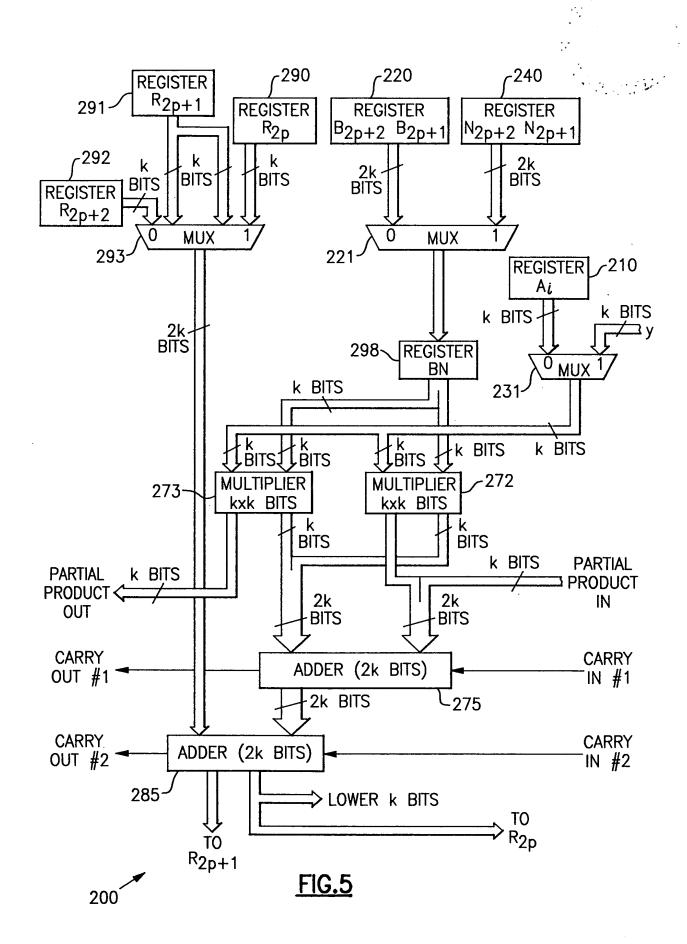
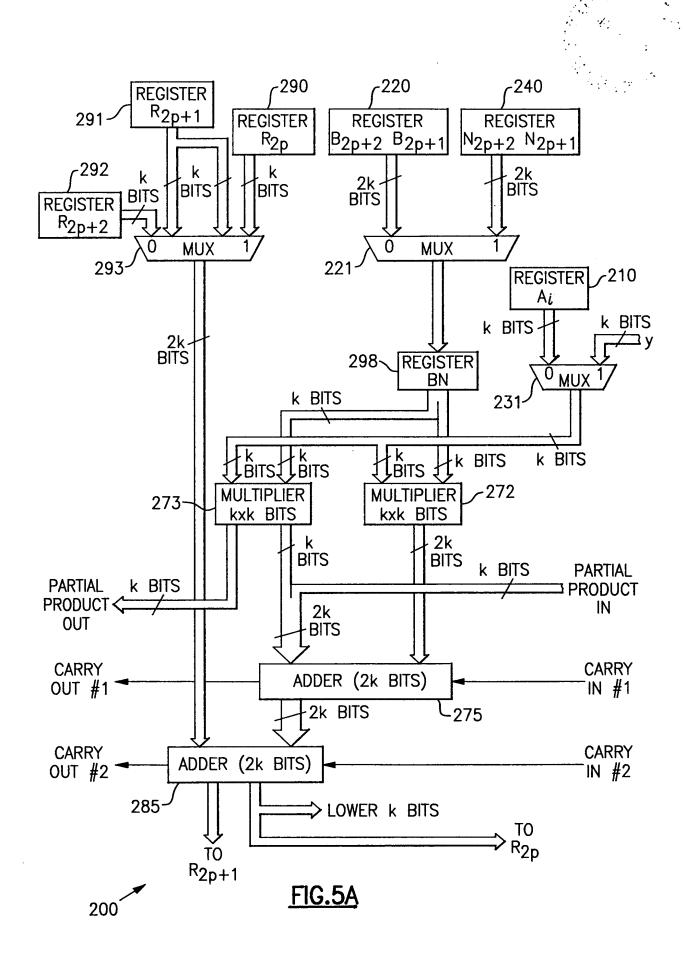


FIG.4

FIG.4A





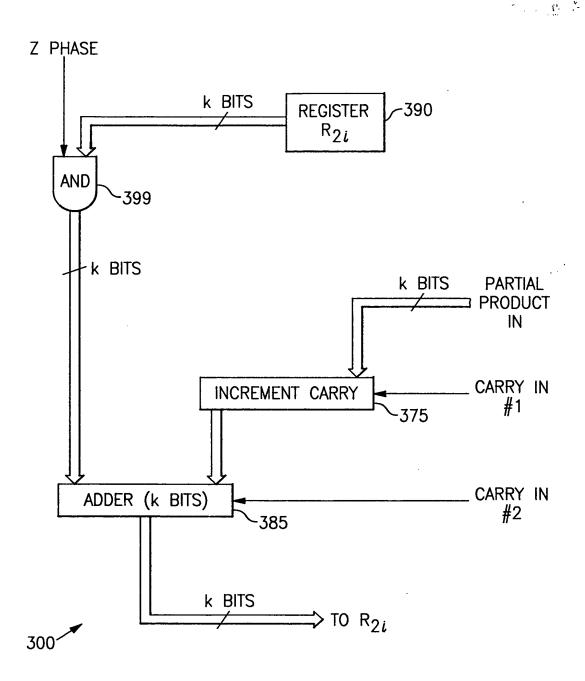
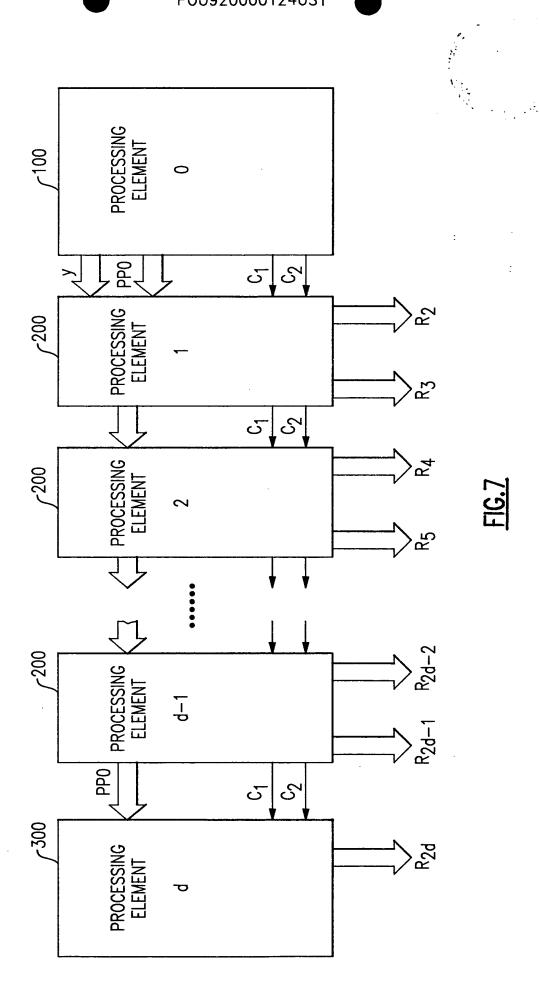
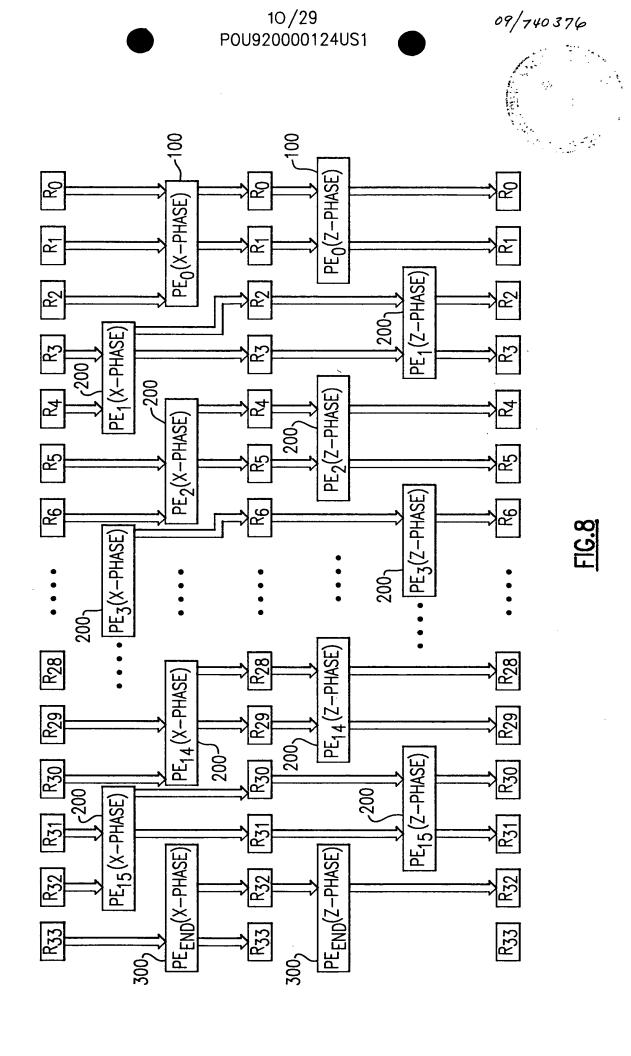
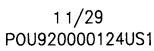


FIG.6







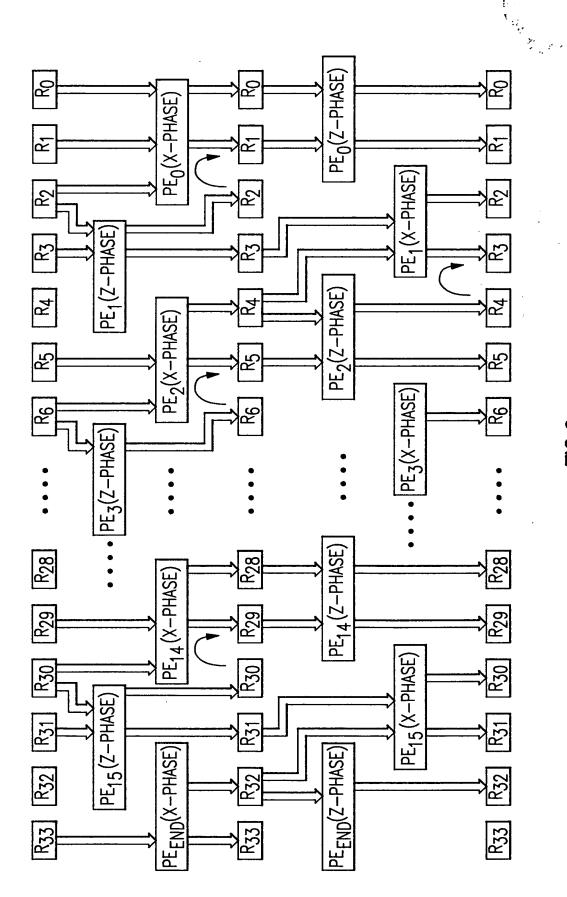
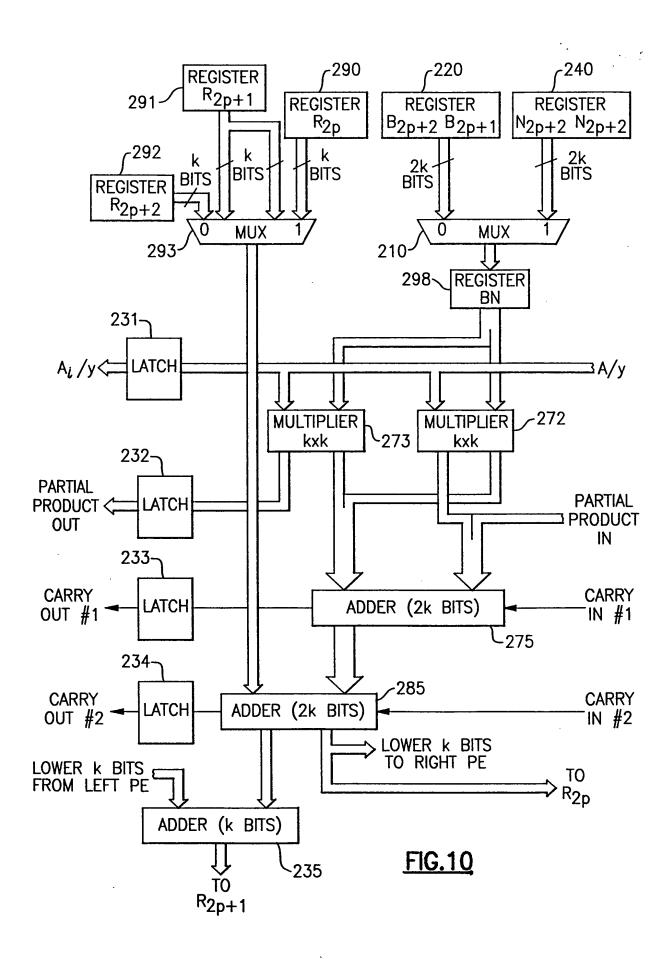


FIG.9



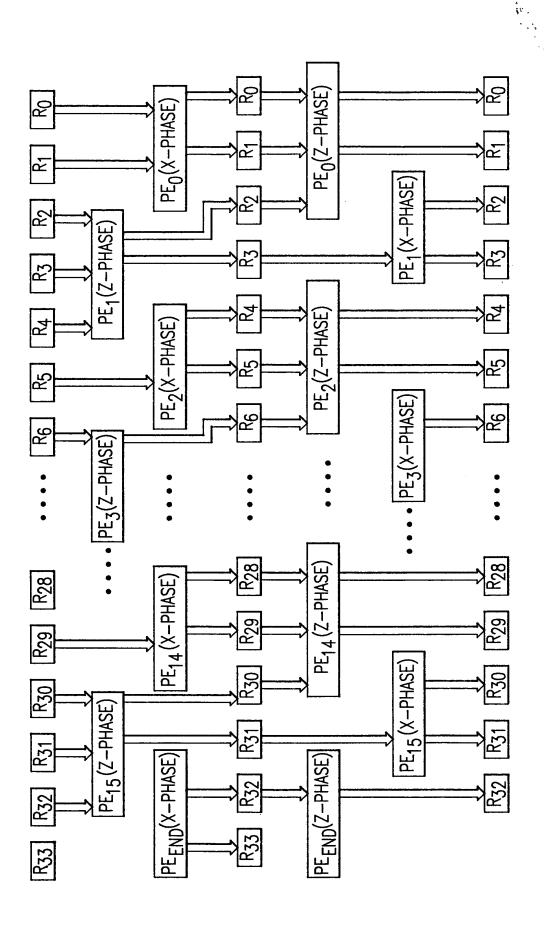
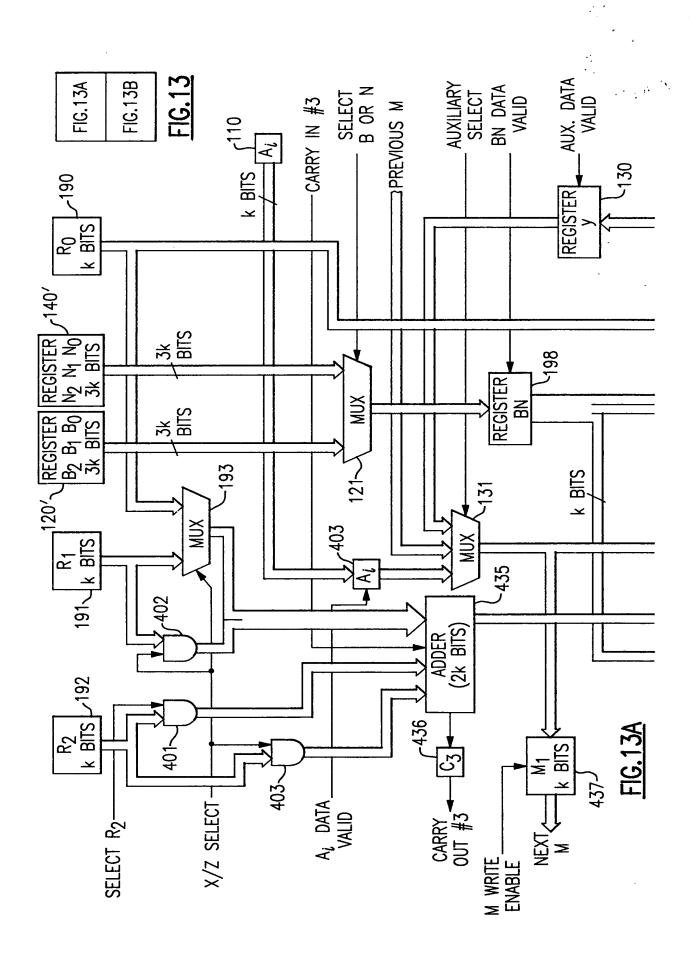
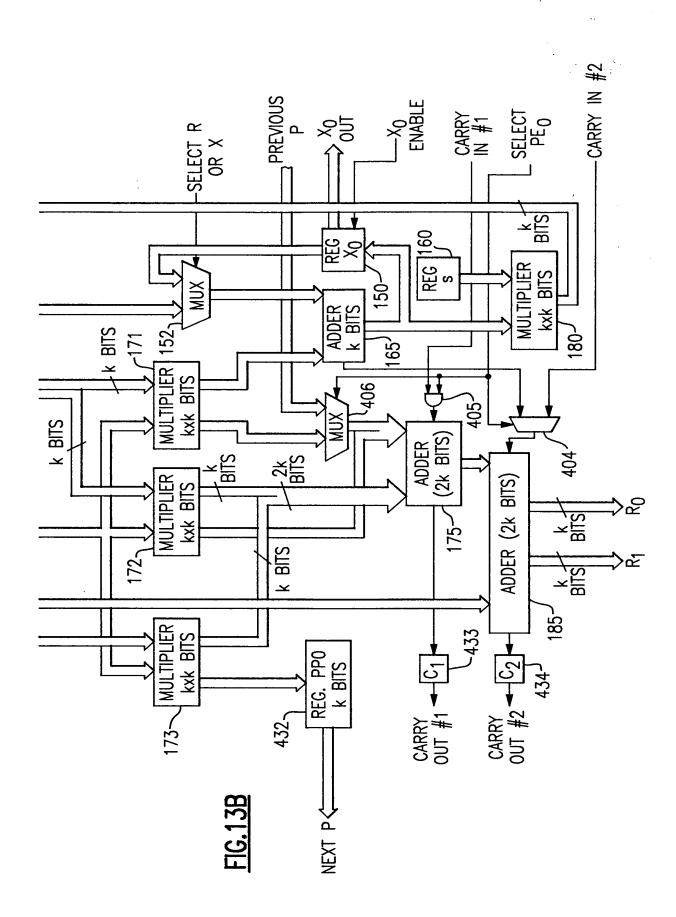


FIG. 12





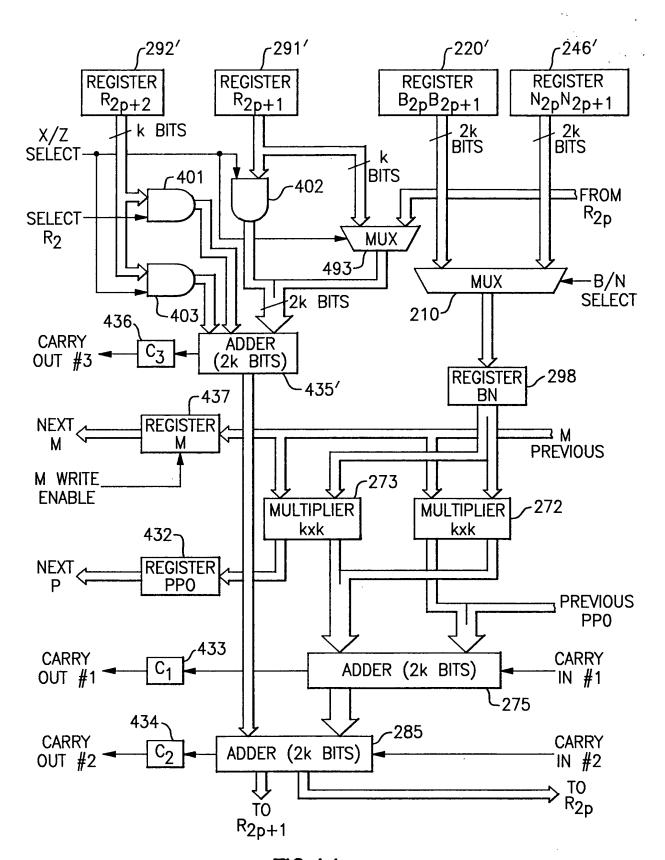


FIG.14

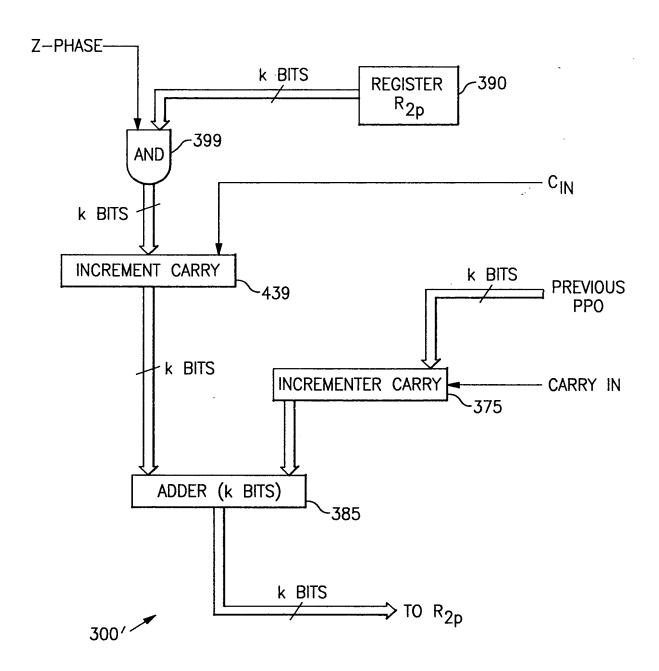


FIG.15

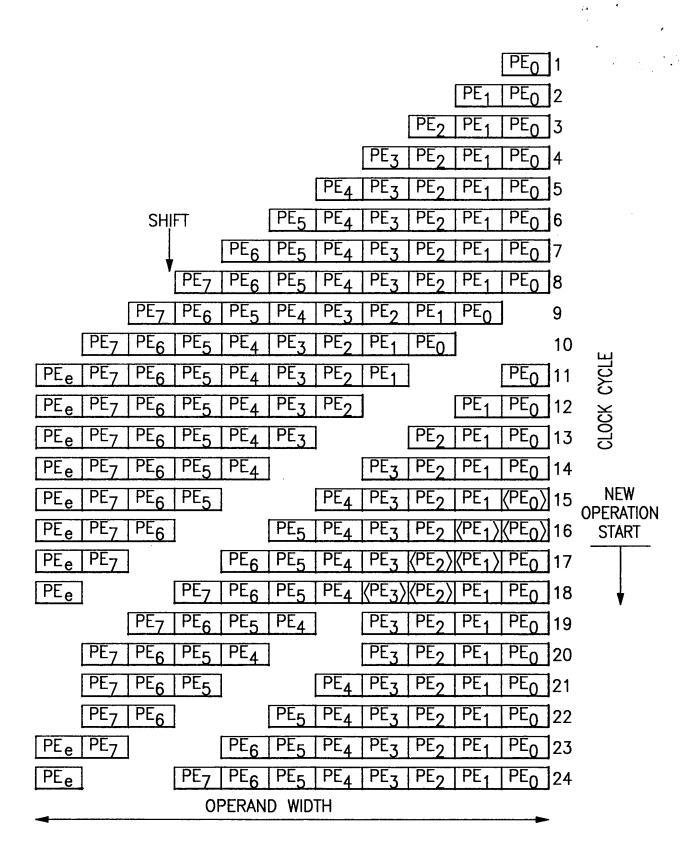
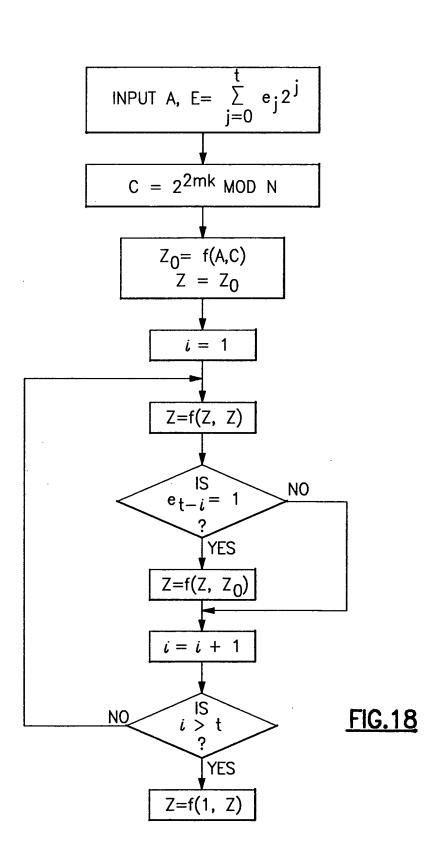


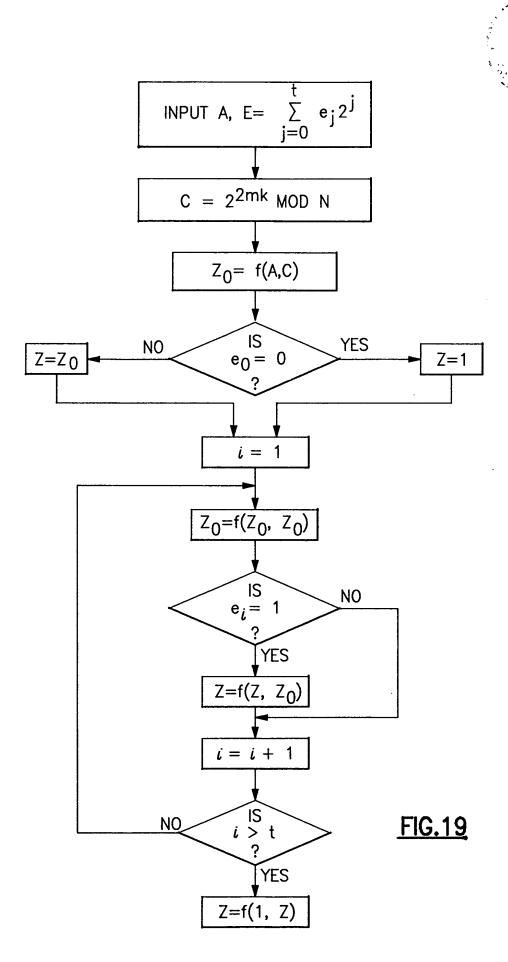
FIG.16

20/29

09/740376

FIG.17





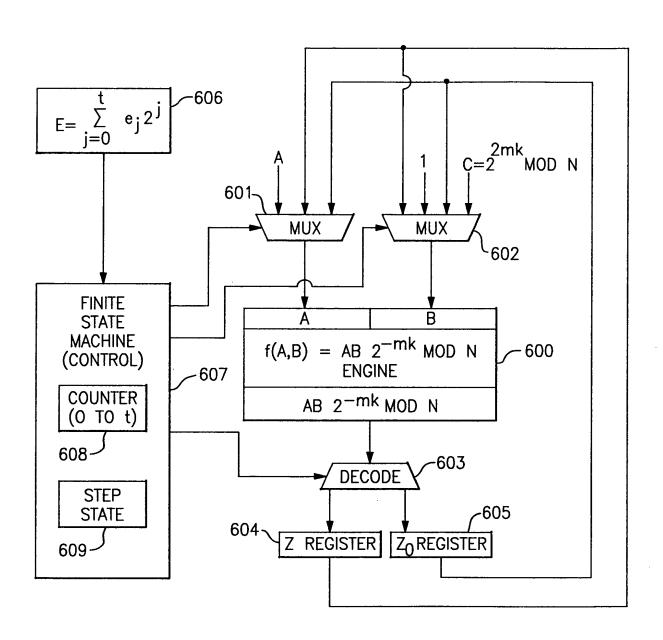
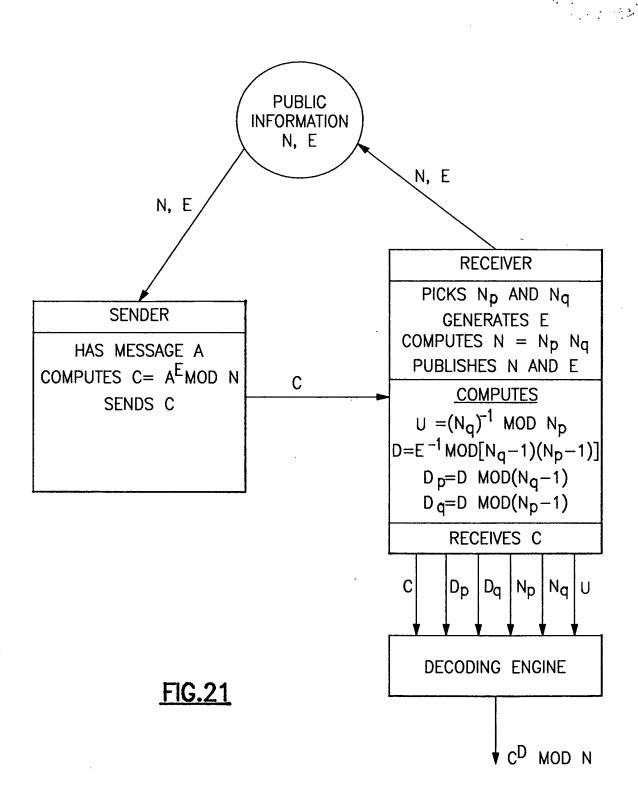


FIG.20



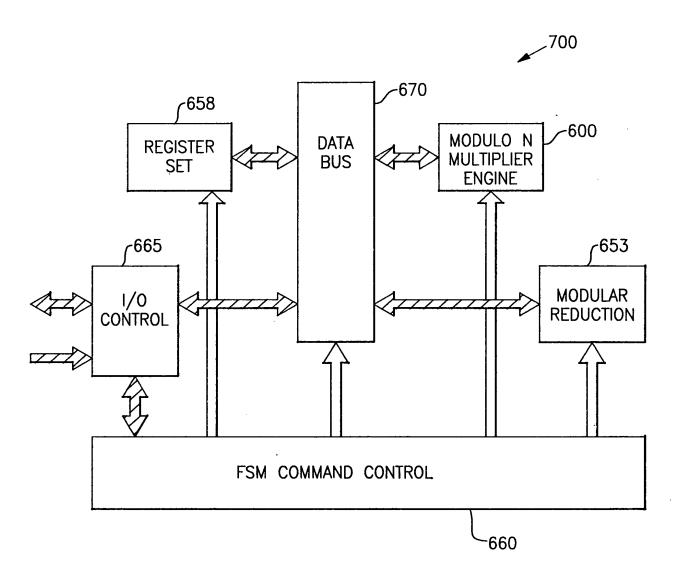
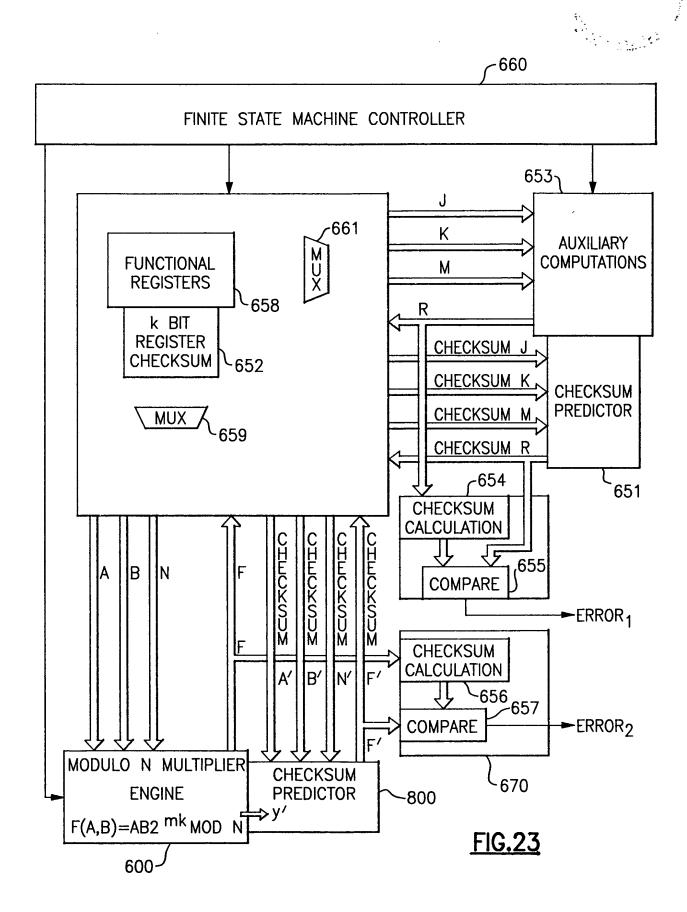


FIG.22



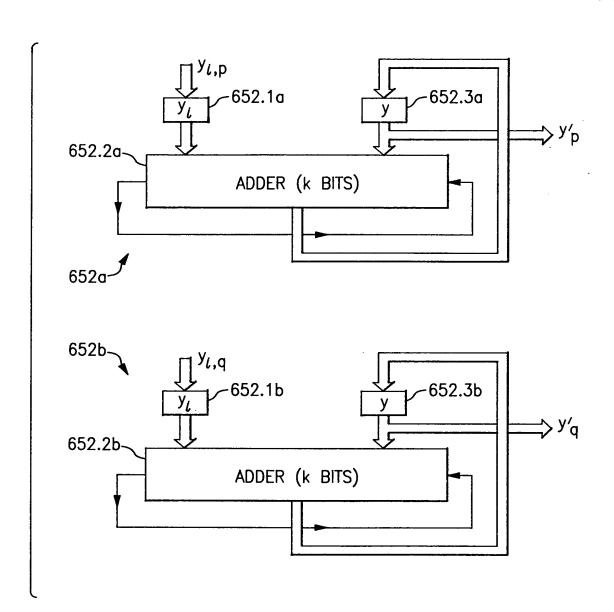


FIG.24

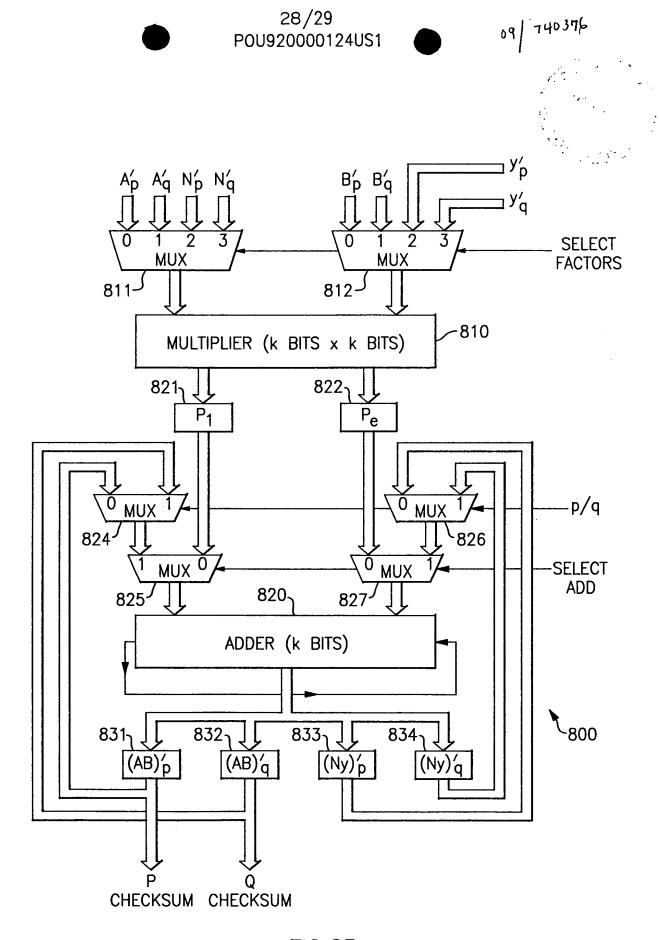


FIG.25

